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Modeling of electrochemical metallization-based two-dimensional material memristors for neuromorphic applications

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***Abstract*—Electrochemical metallization-based two dimensional (2D) material memristors with vertical transport and small inter-electrode distances have been reported recently. Their device characteristics exhibit multiple conductance states with relatively low switching voltages, which make them well-suited for low power neuromorphic applications. Our work models the transport in these 2D material-based memristors, with a focus on explaining and capturing their current-voltage characteristics. The model also captures the dynamics of switching (with an emphasis on the estimation of switching energies and delays), and quantitatively captures the experimentally observed spike-time-dependent plasticity behaviour in these devices. The simulation results obtained using our model (and implemented in Verilog-A) have been validated with experimental data from multiple sources. Our work demonstrates the flexibility of including different transport mechanisms (such as, tunneling, space charge limited conduction) in a unified simulation framework.**

***Index Terms*—dynamic characteristics, electrochemical metallization (ECM), memristors, spike-time-dependent plasticity (STDP), transition metal dichalcogenides (TMDs), two-dimensional (2D) materials.**

I. Introduction

RESISTIVE-SWITCHING devices are a critical component for the realisation of computational systems that mimic biological neural systems. In biological systems, connection weights between the neurons is dependent on the time lapse between the neuron's action potentials. Resistive-switching devices (memristors) with multiple conductance states can mimic this biological spike-time-dependent plasticity (STDP) behaviour, with multiple conductance states being analogous to different synaptic weights. The analog nature observed in the device characteristics is ideal for their use in neuromorphic computing applications, as it mimics the behaviour of a synapse in a neural network that exhibits STDP behaviour [1], [2]. STDP in memristors has been experimentally demonstrated [3]–[14]. Additionally, memristors are one of the contenders as storage elements in non-volatile memories. The change in conductance in memristors can be, broadly, attributed to vacancy migration inside the switching layer (valence change memory: VCM) [6], [7], [9], or to the formation of metallic filaments inside the switching layer (electrochemical metallization: ECM) [4], [8], [13].

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Recently, memristors using two-dimensional (2D) materials, such as MoS_2, WS_2, WSe_2 (transition metal dichalcogenides: TMDs) [4], [8]–[10], [13], [15]–[20] and black phosphorus [21] as switching layers, have been reported. These 2D materials are innately thin and are well-suited for highly scaled devices. Depending on the device structure, the transport in these devices can be vertical [4], [13], [15]–[17], [19], [21], or horizontal [8], [9], [18]. 2D memristors with vertical transport have thin inter-electrode distances and low switching voltages, making them well-suited for low power applications. The resistive switching mechanism in these devices is, usually, VCM [9], [16], [17], or ECM [4], [8], [13], [18], [21]. There have also been reports where the switching is attributed to metal substitution in sulphur vacancies in certain TMD memristors [20]. Since most of these devices exhibit analog switching characteristics with multiple conductance states, they can be configured to exhibit STDP behaviour as well, as demonstrated experimentally in [4], [13].

A wide range of models ranging from simple macro models [22] to atomistic Monte-Carlo models [23] explain resistive switching in ECM devices. Some of these models explain current-voltage (I-V) characteristics based on ion transport and do not include other modes of transport, such as, tunneling [24], [25]. Electron tunneling in ECM devices, along with ion transport, has been modeled in [26], [27]. However, these models have not been developed specifically for 2D material-based memristors. Note that devices with metal-2D material interfaces have low barrier heights [28]–[32]. The estimation of tunnel current in such devices must, therefore, include the possible change of barrier geometry during the input voltage sweep [33]. Moreover, in devices with some 2D materials as switching layers, the impact of space charge limited current (SCLC) has to be considered [4], [13], [21]. A model which incorporates these aspects will be able to capture the behaviour of 2D material-based ECM memristors.

In this work, our focus is to model the static and dynamic characteristics of 2D material-based ECM memristors with vertical transport, for neuromorphic applications. The physics of ion transport in a generic ECM memristor has been given in [26], [27], [34], which captures its I-V characteristics. Recently, we had used this approach to model the I-V and its associated variability in ECM-based TMD memristors [35]. In this paper, we have enhanced this model to accommodate multiple modes of transport in 2D material-based ECM

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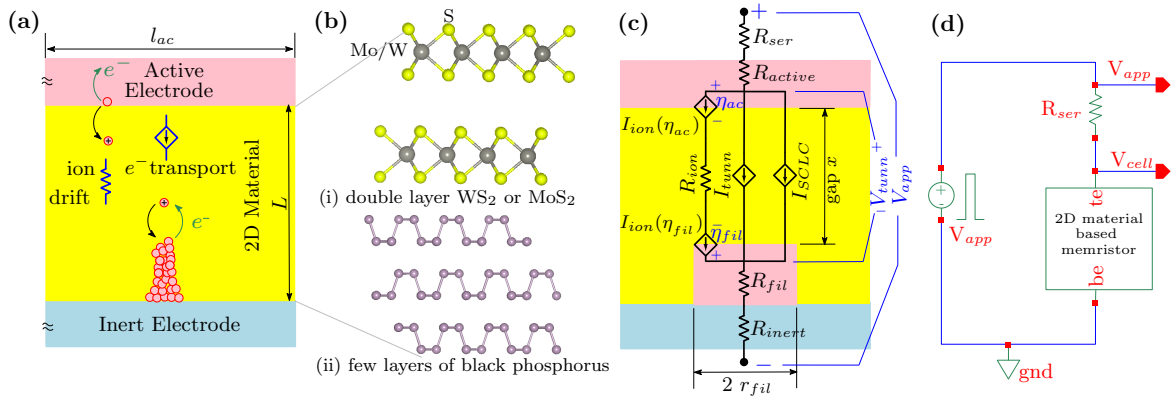

Fig. 1. Schematic of: (a) a typical device structure of an ECM-based 2D memristor, illustrating the various physical processes occurring in the switching layer. (b) layered 2D materials, such as, MoS_2, WS_2, black phosphorous. (c) the equivalent circuit model; the different components in this circuit are discussed in Section II-C. (d) the setup in Cadence Spectre; the 2D material-based memristor block implements the algorithm shown in Fig. 2, using Verilog-A.

memristors (in addition to ion transport) – different tunnel mechanisms that are mainly dependent on the geometry of the barrier profile, and transport based on SCLC. The statics and dynamics of switching in 2D material-based memristors have been simulated with this approach, with an emphasis on the estimation of switching energies and delays. Additionally, we have quantitatively captured the STDP behaviour in these devices using the proposed model (implemented in Verilog-A). Our simulation results are validated with experimental data from multiple sources [4], [13], [21].

This paper is organized as follows. Section II outlines the typical device structure under consideration, followed by presenting our modeling approach along with the relevant approximations. Section III discusses the simulation results of I-V characteristics, accounting for their variability and analog nature, using the proposed model. Section IV discusses the simulation results related to the dynamics of switching along with the estimation of switching energies and delays, and its comparison with experimental data. Section V discusses the simulation results for the STDP behaviour, using the proposed model. Finally, Section VI presents our conclusions.

II. Device Model

A. Device Structure

The schematic of the device structure of a typical 2D material-based memristor along with an illustration of the physical processes that occur during ECM-based switching, is shown in Fig. 1(a). These devices have an active electrode (such as, Cu or Ag), few layers of 2D material as the switching layer, and an inert electrode. A few of the layered 2D materials that have been used as the switching layer in ECM-based memristors with vertical transport [4], [13], [21], are illustrated in Fig. 1(b).

Resistive switching in ECM-based devices is, mainly, due to the redox reactions that occur at the metal-switching layer interfaces, electric field-driven ion migration, and the formation and dissolution of metallic filaments inside the switching layer [36]. During the SET process, nano-sized metallic filaments are formed inside the switching layer, switching the device from a high resistance state (HRS) to a low resistance state (LRS); during the RESET process, these metallic filaments dissolve upon the application of a bias with opposite polarity, switching the device back from LRS to HRS.

B. Model Framework and Approximations

Filament: In ECM-based devices with large dimensions of electrodes, growth of multiple filaments inside the switching layer is likely, due to multiple redox reactions that occur at the metal-switching layer interfaces. The growth rate of each of these filaments will be different. In this model, all calculations are made considering the fastest growing filament; that is, the calculation of the current in the device considers the growth of a single filament only. This is reasonable since tunneling current is exponentially dependent on the gap between the filament and the contact. Therefore, the current in the device will be dominated by the current from the fastest growing filament, effectively.

Even though filaments can have arbitrary geometrical shapes, we have assumed that they are cylindrical. Additionally, within a few cycles of measurement, we have assumed that the axial growth of the filament is more dominant as compared to its lateral growth; thus resulting in the formation and dissolution of a cylindrical filament with constant radius. The in-situ characterization of ECM memristors has shown that the filaments are nearly cylindrical or conical in shape [37], [38]. Therefore, cylindrical filament growth in devices with very thin switching layers (as is the case here), is a reasonable assumption.

Ion transport: In the presence of an electrical input, metal ions can hop through barriers, which can be interstitials or vacancies [4], [20], [39]. For the 2D material-based ECM memristors under consideration, since the applied electric field (E) is mostly less than the characteristic electric field for mobile ions in the switching layer (E_0) at room temperature, nonlinear ion hopping is approximated to linear ion drift [40]; this is discussed in Section II-C.

Electron transport: Since the thickness of the switching layer is small (therefore, the gap between the filament and the active electrode is smaller), tunnel current is one of the

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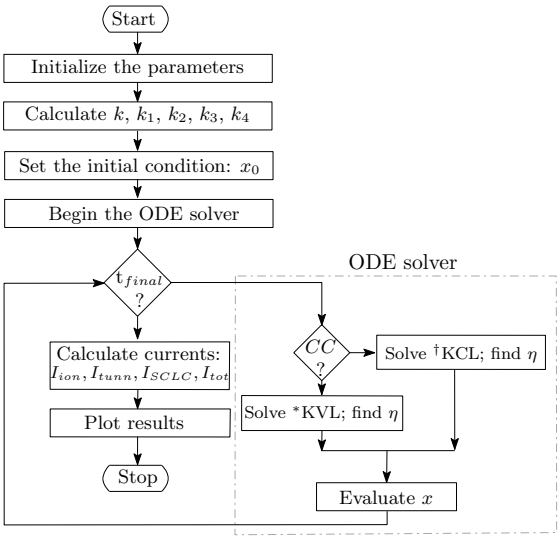

Fig. 2. Flowchart indicating the simulation procedure.
CC is the current compliance; t_{final} is the final time instant of simulation. †KCL: Kirchhoff's current law. *KVL: Kirchhoff's voltage law.

dominant modes of electron transport in these devices. Transmission coefficients in the tunnel current, have been calculated using the WKB approximation. The *Fermi-Dirac* function has been replaced by a step function, to avoid numerical integration (*zero-temperature* approximation) [41], [42]. Additionally, since tunnel current densities calculated by accounting for confinement in nano-sized filaments and those that have been calculated without accounting for any confinement do not deviate substantially even when the filament-diameters are small [43], we have not accounted for any confinement in these filaments. Different tunnel mechanisms are dominant for different barrier profiles, which is discussed in Section II-C.

For the 2D material-based ECM memristors under consideration [4], [13], [21], the electrons injected from the electrodes tend to accumulate near the defect sites in the switching layer, thus forming a region of space charge. The impact of space charge limited current (SCLC) on the I-V characteristics of the device is dependent on the thickness and quality of the switching layer [44]–[46]. The influence of SCLC on the device characteristics of different 2D material-based memristors is analysed in Section III.

While these assumptions and approximations abstract some details of the ECM process, we find that it presents a good description of the static and dynamic characteristics of many experimentally fabricated 2D material-based ECM memristors, as shown in Sections III, IV, and V. We also anticipate that this simple approach will be most amenable for the simulation of large arrays of these devices.

C. Modeling Approach

Fig. 1(c) shows the schematic of the equivalent circuit. The total current through the device I_{tot} [Eq. (1)] consists of an ionic component I_{ion} [*see* Eq. (2)]; and two electronic current components: (a) a tunnel component I_{tunn}, which is very sensitive to the tunnel gap x, and the barrier height $q\Phi_0$ [*see* Eq. (6) and (7)]; and (b) a space charge limited current

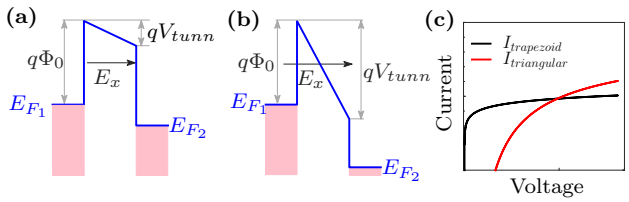

Fig. 3. (a)-(b) Schematic of the energy band profile showing the metal-2D material-metal interface, in the case of: (a) a trapezoidal barrier. (b) a triangular barrier. (c) Current through the different barriers.

(SCLC) component I_{SCLC}, which depends on the properties of the switching layer and the gap x [*see* Eq. (8)].

$$I_{tot} = I_{ion} + I_{tunn} + I_{SCLC} \tag{1}$$

The ionic current drives the ECM process, which involves a charge transfer reaction. This is described by the *Butler-Volmer* equation [26], [27],

$$I_{ion} = I_0 \left\{ \exp\left(z\frac{q}{k_B T}(1-\alpha)\eta \right) - \exp\left(-z\frac{q}{k_B T}\alpha\eta \right) \right\} \tag{2}$$

where, I_0 represents the exchange current, α is the charge transfer coefficient, z is the charge transfer number, η is the overpotential at the metal-switching layer interface, k_B is the Boltzmann constant, and T is the temperature.

The applied voltage, V_{app}, drops across the tunnel gap (V_{tunn}), metallic filament ($I_{tot} \cdot R_{fil}$), the top and bottom electrodes [$I_{tot} \cdot (R_{active} + R_{inert})$], and a series resistance ($I_{tot} \cdot R_{ser}$):

$$V_{app} = V_{tunn} + I_{tot} \cdot (R_{fil} + R_{active} + R_{inert} + R_{ser}) \tag{3}$$

R_{ser} can be attributed to contact resistance, and/or to the introduction of a series resistance to limit the current through the device. The filament resistance, R_{fil}, is calculated as $R_{fil} = \rho_{fil} \cdot (L - x)/(\pi r_{fil}^2)$, where r_{fil} is the radius of the filament.

The total voltage drop across the tunnel gap is given by,

$$V_{tunn} = \eta_{ac} + (I_{ion} \cdot R_{ion}) - \eta_{fil} \tag{4}$$

where, η_{ac} and η_{fil} are the overpotentials at the active electrode-switching layer interface and the filament-switching layer interface, respectively. R_{ion} is the ion resistance, calculated as $R_{ion} = \rho_{ion} \cdot x/(\pi r_{ion}^2)$. Here, we assume $r_{ion} = r_{fil}$.

The change in tunnel gap, x, due to filament growth and dissolution is given by *Faraday's law* of electrolysis [26], [27]:

$$\frac{dx}{dt} = -k \cdot J_{ion}, \quad \text{where,} \quad k = \frac{M_{Active}}{z \cdot q \cdot \rho_{m_{Active}}} \tag{5}$$

J_{ion} is the ionic current density; M_{active} and $\rho_{m_{active}}$ are the the atomic mass and mass density of active electrode, respectively.

As the metal-2D material interfaces have low barrier heights, during the input sweep, the barrier profile can change from trapezoidal [for lower voltages: when $qV_{tunn} < q\Phi_0$; *see* Fig. 3(a)] to triangular [for higher voltages: when $qV_{tunn} > q\Phi_0$; *see* Fig. 3(b)]. We have accounted for both cases [35].

TABLE I
NOMINAL PARAMETER VALUES USED FOR SIMULATIONS

Parameters	**Cu/MoS_2/Au [4]**	**Ag/WS_2/Pt [13]**	**Cu/BP/Au [21]**	**Remarks**
Mass density of active electrode, $\rho_{m_{active}}(\times 10^6 g/m^3)$	8.95 [26]	10.49 [27]	8.95 [26]	material parameter of the active electrode
Atomic mass of active electrode, $M_{active}(\times 10^{-22} g)$	1.06 [26]	1.79 [27]	1.06 [26]	material parameter of the active electrode
Ion resistivity, $\rho_{ion}(\Omega - m)$	1×10^{-2} [26]	1×10^{-2} [26]	1×10^{-2} [27]	ρ_{ion} in switching layer, fitting parameter
Filament resistivity, $\rho_{fil}(\times 10^{-8}\Omega - m)$	2 [26], [47]	1.8 [27]	2 [26], [47]	material parameter of the metal filament
Charge transfer number, z	2 [26]	1 [27]	2 [26]	material parameter of the active electrode
Exchange current density, $j_0(A/m^2)$	8×10^{-2}	2×10^4	4×10^{-2}	depends on temperature, ion concentration [26]; fitting parameter
Active electrode resistivity, $\rho_{active}(\Omega - m)$	1.7×10^{-8} [48]	1.6×10^{-8} [48]	1.7×10^{-8} [48]	material parameter of the active electrode
Inert electrode resistivity, $\rho_{inert}(\Omega - m)$	2.4×10^{-8} [48]	0.98×10^{-7} [48]	2.4×10^{-8} [48]	material parameter of the inert electrode
Switching layer thickness, $L(\times 10^{-9} m)$	1.23 [4]	65 [13]	15, 32 [21]	determined by the device under consideration
Tunnel barrier height, $q\Phi_0(eV)$	0.5 [28], [29]	0.38 [31], [32]	0.55 [30]	based on metal-switching layer interface
Temperature, $T(K)$	300 [4]	300 [13]	300 [21]	determined by measurement temperature
Effective mass of electron, m_{eff}	$0.55m_0$ [49]	$0.37m_0$ [50]	$0.20m_0$ [51]	m_{eff} in switching layer; material parameter
Mobility of electrons, $\mu(m^2/Vs)$	270×10^{-4} [52]	40×10^{-4} [53]	1.10 [54]	μ in switching layer, material parameter
Dielectric constant, ϵ_r	4 [55]	6.6 [56]	3.06 [57]	ϵ_r of switching layer, material parameter
Free charge carrier fraction, θ	8×10^{-4}	8×10^{-4}	16×10^{-2}	fraction of free electrons from injected ones; fitting parameter

The tunnel current through different barriers, at different bias regimes, is depicted in Fig. 3(c).

The tunnel current, at low bias, through a trapezoidal barrier, can be approximated as [26], [27], [33], [42]:

$$I_{trapezoid} \approx \frac{k_1}{x} \cdot V_{tunn} \cdot \exp\left(-\frac{4\pi}{h} k_2 x\right) \tag{6}$$

where, $k_1 = \pi r_{fil}^2 \cdot \frac{3q^2 C k_2}{2h^2}$, $k_2 = \sqrt{2m_{eff}\Phi_0}$, and m_{eff} is the effective mass of the electron in the switching layer.

The tunnel current across a triangular barrier is given by [41], [33]:

$$I_{triangular} \approx \frac{k_3}{x^2} \cdot V_{tunn}^2 \cdot \exp\left(-\frac{k_4 x}{V_{tunn}}\right) C_1 \tag{7}$$

where, $k_3 = \pi r_{fil}^2 \cdot \frac{q^3 m_e}{8\pi m_{eff} h (q\Phi_0)}$, $k_4 = \frac{8\pi\sqrt{2m_{eff}}}{3hq} \cdot (q\Phi_0)^{\frac{3}{2}}$,

$$C_1 = 1 - [(\lambda \cdot qV_{tunn}) + 1] \exp\{-\lambda \cdot qV_{tunn}\},$$

and $$\lambda = \frac{4\pi\sqrt{2m_{eff}}}{hq} \cdot \frac{x}{V_{tunn}} \cdot (q\Phi_0)^{\frac{1}{2}}$$

SCLC is a function of both, the gap x and the tunnel voltage V_{tunn}. It is modeled as a voltage-controlled current source I_{SCLC}, as shown in Fig. 1(c), and given by [44]–[46]:

$$I_{SCLC} = \theta \cdot \epsilon \cdot \mu \cdot \frac{V_{tunn}^2}{x^3} \left(\pi r_{fil}^2\right) \; ; \theta = \frac{9}{8} \cdot \frac{n_{free}}{n_{free} + n_{trap}} \tag{8}$$

θ is the ratio of free carriers to total carriers injected, n_{free} and n_{trap} represent free and trapped carrier densities, respectively. ϵ_r is the dielectric constant of the switching layer and μ is the mobility of electrons in the switching layer [44]–[46].

Based on the switching layer thickness, each transport mechanism has a different impact on the switching characteristics. In general, the ion current influences the SET voltage. As the ion current increases, filament grows at a faster rate, and hence, the SET voltage decreases [26]. Tunnel current is dominant in both LRS and HRS for devices with thin switching layers. However, for devices with comparatively thicker switching layers, other components, such as SCLC can be dominant in HRS; this is because the tunnel current decreases exponentially with increasing tunnel gap. Our model has been validated with multiple experimental data in [4], [13], [21], discussed in detail in Section III.

III. SIMULATION OF I-V CHARACTERISTICS

The simulations of I-V characteristics of 2D material-based ECM memristors are presented in this section. An explicit *Runge-Kutta* method, implemented in MATLAB, is used for solving the ordinary differential equation, Eq. (5) [35]. In this work, we have implemented the proposed model using Verilog-A as well, which gives identical results. The Verilog-A approach is simpler to use while simulating circuits involving memristors. Fig. 1(d) shows the simulation setup in Cadence Spectre, and Fig. 2 explains the simulation procedure. The nominal values of the parameters used for simulation, along with justifications, are summarised in Table I.

A. I-V in pristine devices

In this section, simulation of initial I-V characteristics of different 2D material-based memristors using the proposed model is presented. Initially, we consider Cu/MoS_2/Au memristor, whose device structure and detailed fabrication procedure are given in [4]. The I-V of pristine devices with

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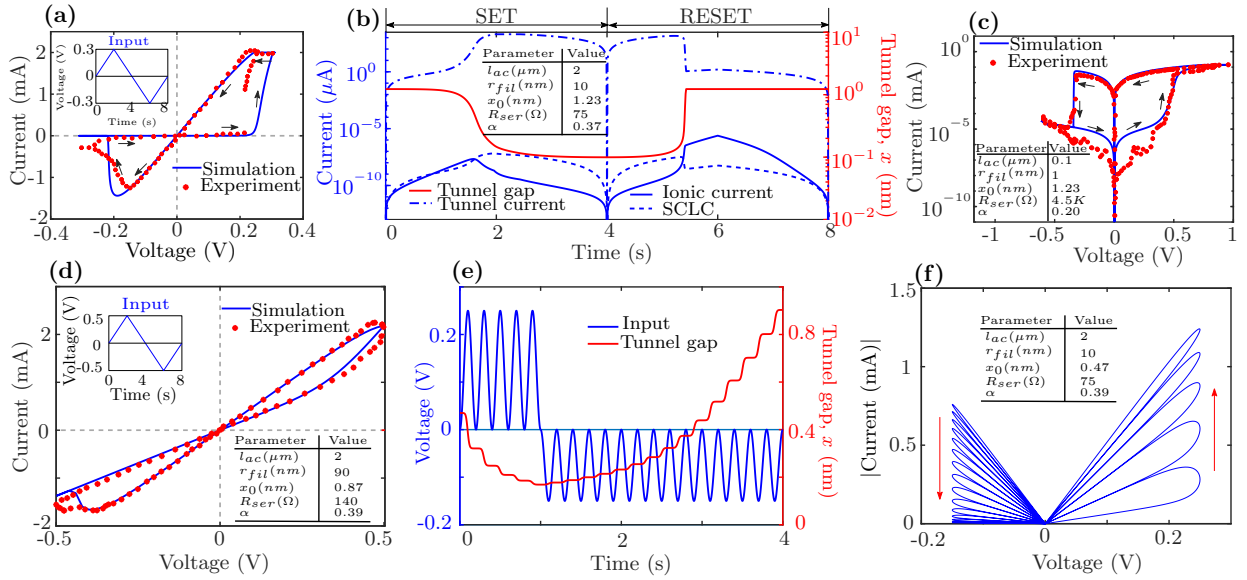

Fig. 4. Simulation of Cu/MoS_2/Au memristor: (a), (b), (d)-(f) Simulation results for device with $2\mu m \times 2\mu m$ area: (a) I-V characteristics of a pristine device, with current compliance at $2mA$; inset shows the input voltage. (b) Variation of tunnel gap and different current components, as a function of the time-step corresponding to the input bias shown in the inset of (a). (d) Variability in I-V, due to the existence of a residual and changing filament. (e)-(f) Multiple conductance states: (e) Consecutive positive and negative input cycles, and corresponding changes in the tunnel gap. (f) I-V characteristics. (c) Simulation results of I-V characteristics for a pristine device with $0.1\mu m \times 0.1\mu m$ area; high value of R_{ser} indicates the use of a current-limiting resistor. (a)-(f) All experimental data is from [4]; parameter values used for the simulation are given in respective insets and in Table I.

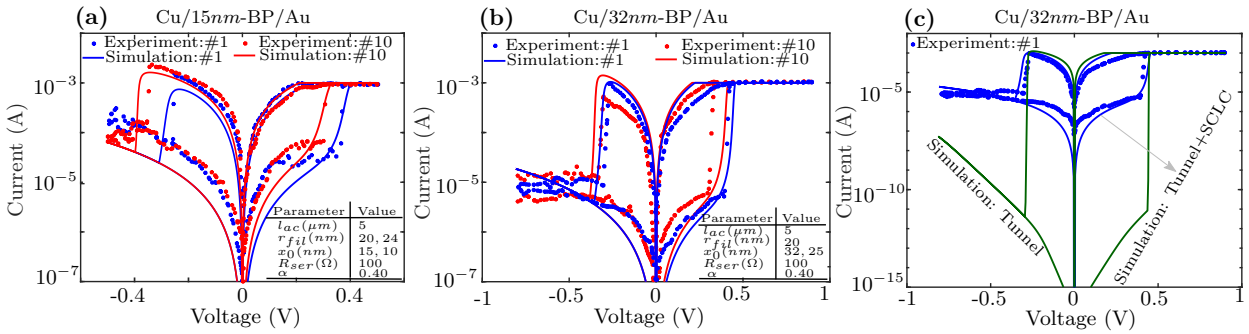

Fig. 5. Simulation of I-V characteristics of Cu/BP/Au memsitor: (a) with $15nm$-thick BP. (b) with $32nm$-thick BP. The experimental and simulation data shown correspond to the first and tenth cycle of measurement. (c) with $32nm$-thick BP, SCLC is found to be more dominant than the tunnel current, specially in the HRS regime. All experimental data is from [21]; parameter values used for the simulation are given in respective insets and in Table I.

different electrode areas have been simulated and compared with experimental data, and are shown in Fig. 4(a)-(c). The parameter values used for the simulation are listed in Table I and in the insets of Fig. 4(b) and (c). In pristine devices, the initial gap between the filament and the top electrode is almost equal to the thickness of the switching layer; that is, the filament thickness, initially, is negligible. When the device undergoes multiple SET and RESET cycles, a small residual filament can remain, leading to different initial filament thickness for further voltage cycles. The input signal used for the simulations is shown in the inset of Fig. 4(a), and is consistent with the measurement setup used in [4]. The variation of the tunnel gap and different current components, as a function of time, is shown in Fig. 4(b). A decrease in the tunnel gap increases the tunnel current, and the device switches from HRS to LRS (SET); an increase in the tunnel gap (as seen in the latter half of the input cycle) leads to decreasing tunnel current, switching the device back to HRS (RESET). Due to the thin MoS_2 switching layer, the tunnel current is always higher (by orders of magnitude) than the ionic and SCLC components.

We have also considered black phosphorous (BP)-based ECM memristors, whose device structure and fabrication details are reported in [21]. Note that the switching layer is thicker in these devices, as compared to the MoS_2 memristors discussed earlier. The simulated I-V characteristics of pristine Cu/$15nm$-BP/Au and Cu/$32nm$-BP/Au memristors are shown in Fig. 5(a) and (b), respectively, and is compared with the corresponding experimental data obtained from [21]. The parameter values used for the simulation are listed in Table I and in the insets of Fig. 5(a) and (b). In these devices, SCLC is found to be more dominant than the tunnel current, specially in the HRS regime; this is clearly seen in Fig. 5(c). The impact of SCLC is significantly higher in these devices, as compared to MoS_2 memristors discussed earlier.

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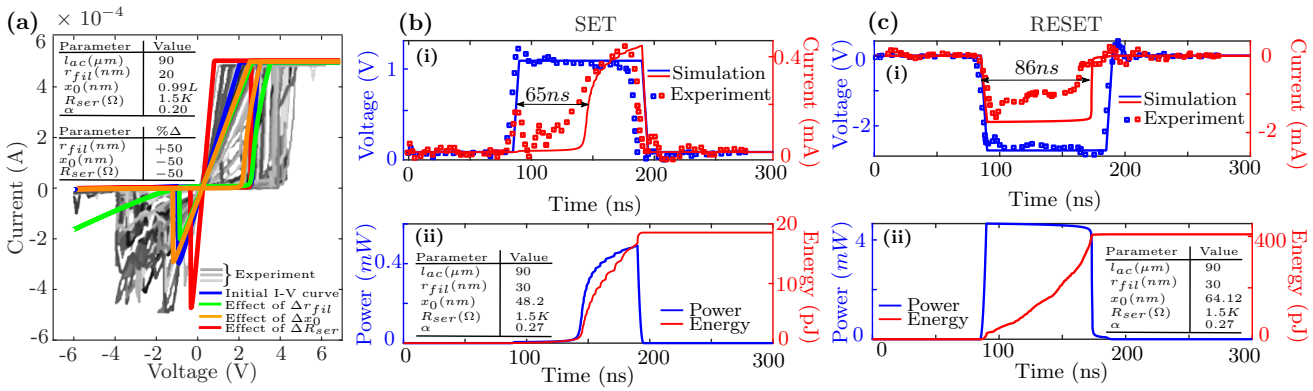

Fig. 6. (a) Simulation of I-V characteristics of Ag/WS_2/Pt memristors. Δ indicates the change in the values of the parameters from those used during the initial run; this captures the variability in I-V. Traces in different shades of grey in the background show the experimentally measured I-V and its associated variability during multiple input sweeps. (b)-(c) Simulation results for the dynamics of the switching during: (b) SET process. (c) RESET process. All experimental data is from [13]; parameter values used for the simulation are given in respective insets and in Table I.

B. Variability and analog nature

In this section we analyze the capability of our model in explaining the intra-device variability of different memristors. Our analysis shows that the presence of residual and changing filaments in the switching layer, significantly impacts the intra-device variability. Additionally, this explains the analog nature of the device, which is essential for neuromorphic applications.

As observed experimentally in Cu/MoS_2/Au memristors [4], after multiple input cycles, the resistance observed in HRS is smaller than the corresponding resistance for a pristine device. This variability in I-V, after repeated input sweeps, can be attributed to the incomplete dissolution of the filament after each cycle. Fig. 4(d) shows the simulation results for I-V characteristics, with non-zero initial filament thickness and increased filament diameter (as compared to the corresponding pristine device). The parameters used for the simulation are given in Table I and in the inset of Fig. 4(d). Upon the application of consecutive positive and negative input voltage pulses, multiple conductance states have been observed in these devices [4]. The simulation results are shown in Fig. 4(f). Variation of the tunnel gap as a function of time and applied voltage, is shown in Fig. 4(e). With consecutive positive(negative) bias cycles, increase(decrease) in conductance is observed along with the collapse of the hysteresis window; this is due to the gradual reduction(increase) in the tunnel gap [*see* Fig. 4(e) and (f)]. Our model is able to capture the qualitative behaviour of experimentally measured characteristics in [4].

Variability has also been experimentally observed in Ag/WS_2/Pt [13] and Cu/BP/Au memristors [21], after multiple input sweep cycles. Our model is able to capture the variability in these devices as well, by considering a non-zero initial filament length and increased filament radius (due to residual and changing filaments), and change in the effective series resistance (due to change in interface resistance). The variability in Cu/BP/Au and Ag/WS_2/Pt memristors are simulated and shown in Fig. 5(a)-(b) and Fig. 6(a), respectively.

The parameters used for the simulation are listed in Table I and in the insets of the respective figures. Our model is thus able to capture the experimentally measured I-V characteristics and the associated variability reasonably well, and across multiple ECM-based memristors with different 2D materials used as switching layers.

IV. Simulation of the Dynamics of Switching

In this section, the simulation of the switching characteristics during dynamic SET and RESET processes is explained using the proposed model. Further, we estimate the switching energies and delays during SET and RESET processes using the simulation results, and validate with experimental data from literature. Estimation of these parameters is crucial for the use of memristive devices in both, memory and neuromorphic applications. This is essential in predicting the power budget of arrays of the device under consideration, before proceeding with the fabrication and implementation of these systems.

We have simulated the dynamics of switching in Ag/WS_2/Pt memristors, fabricated in [13]. The model for the Ag/WS_2/Pt memristor is implemented in Verilog-A using Cadence Spectre, and the corresponding circuit symbol is created using the schematic editor; the simulation setup is shown in Fig. 1(d). We have used a piecewise linear voltage source, to define the input signal. The simulation procedure is given in Fig. 2. The differential equation is solved numerically in Spectre. At every time-step, node voltages and branch currents are calculated by solving Eq. (3) in voltage-controlled mode, or Eq. (1) in current-controlled mode. Table I gives the nominal parameter values used for simulation.

A. Switching delays during SET and RESET

The simulation results for the switching behaviour during SET and RESET processes are given in Fig. 6(b) and (c), respectively, for the Ag/WS_2/Pt memristors fabricated in [13]. The amplitude of the input pulse used during SET and RESET operation is about $1.1V$ and $-2.7V$, respectively, with pulse duration of about $100ns$, and rise and fall times of about $5ns$. This is consistent with the input signals used for pulsed measurements in the experimental setup detailed in [13]. The device switches from HRS to LRS in about $65ns$ after the SET pulse, and it switches from LRS to HRS about $86ns$

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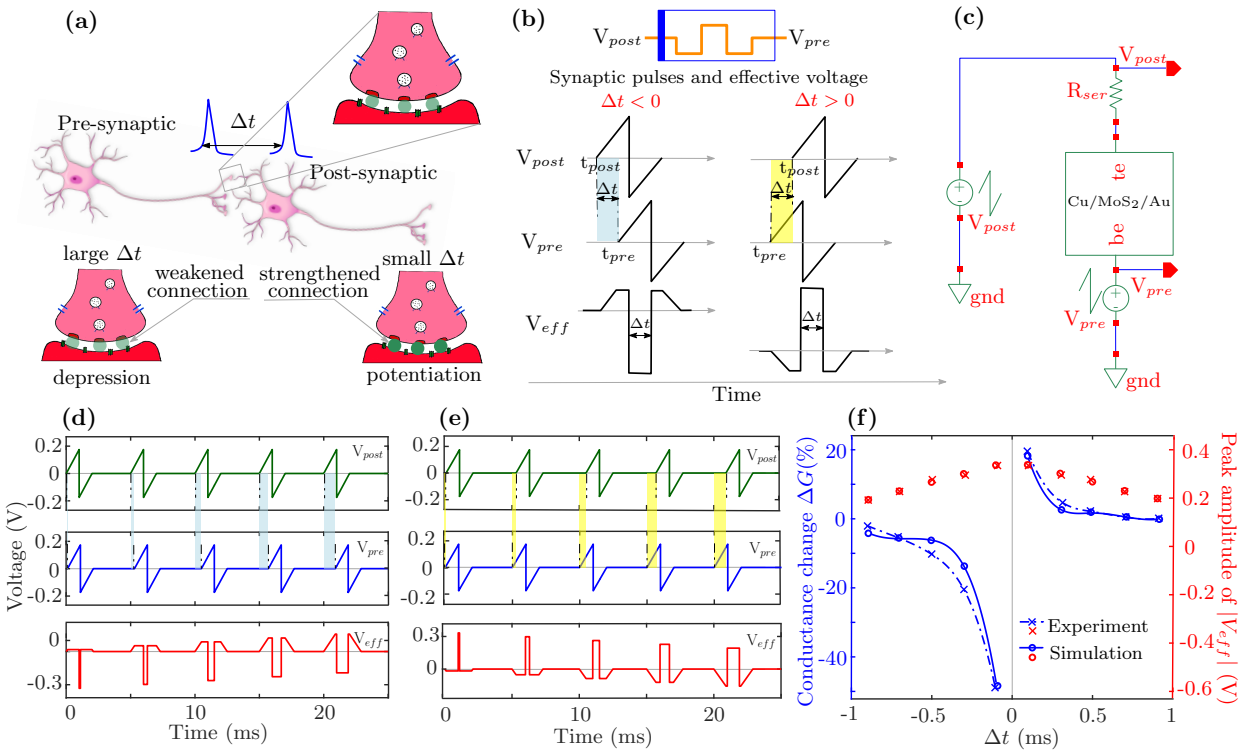

Fig. 7. (a) Illustration of synaptic transmission in neurons. The connection weights between the neurons is dependent on the time lapse between the neuron's action potentials, and this dictates whether the connection between them is strengthened (potentiation), or weakened (depression). This behaviour is called spike-time-dependent plasticity (STDP). (b) The memristive equivalent, with a series of identical pre-synaptic (V_{pre}) and post-synaptic pulses (V_{post}) with a time delay. (c) Setup in Cadence Spectre; the Cu/MoS_2/Au block implements the algorithm shown in Fig. 2, using Verilog-A. (d)-(e) V_{post}, V_{pre}, and V_{eff}, as a function of time, for: (d) $\Delta t < 0$, and (e) $\Delta t > 0$. (f) Simulation results for the variation of the normalized change in conductance (ΔG) as a function of Δt (shown as $\circ$), along with the peak amplitude of $|V_{eff}|$; this has been compared with the experimental data (shown as $\times$) from [4]. *Note:* The lines joining the datapoints ($\circ, \times$) are only a guide for the eye.

after applying the input RESET pulse, which is consistent with the experimentally measured delays during SET and RESET processes in [13].

B. Energy consumption during switching

We have calculated the switching energy during SET and RESET processes. Using the applied voltage (V_{app}) and the cell current (I_{cell}), the instantaneous power (P_{ins}) and switching energy (E_{switch}) are calculated using Eq. (9) and (10), respectively [58].

$$P_{ins}(t) = I_{cell}(t) \times V_{app}(t) \tag{9}$$

$$E_{switch}(t) = \int_0^t I_{cell}(t) \times V_{app}(t) \times dt \tag{10}$$

The switching energy during the SET process is estimated to be about $19pJ$, and the energy consumption during the RESET process is about $406pJ$. The parameter values used for the simulation are listed in Table I and in the insets of the respective figures. Note that the energy consumption during switching is dependent on the peak amplitude and duration of the input pulse; that is, higher the magnitude or/and longer the duration of the SET/RESET pulse, higher is the corresponding switching energy [59], [60].

Estimation of SET and RESET switching delays, switching energies, and power consumption for a single memristor can be useful, as it can be extended to calculate and estimate these parameters (and their limits) in crossbar array architectures of these devices. The expected energy consumption per synaptic event (change from one conductance state to another) in a memristive synapse system is of the order of pJ, which is smaller as compared to that of a synapse system implemented using conventional CMOS technology, which has energy consumption typically in the order of nJ [61]. Thus, our model can be extended to provide useful insight into the design of memristive device arrays for neuromorphic applications.

V. Simulation of STDP Behaviour

A. Review of STDP: pre-synaptic and post-synaptic pulses

In biological systems, connection weights between neurons is dependent on the time lapse between the neuron's action potentials. This behaviour is called spike-time-dependent plasticity (STDP), illustrated in Fig. 7(a). Memristors with multiple conductance states can mimic this biological STDP behaviour, with multiple conductance states being analogous to different synaptic weights. This can be achieved by the application of a series of identical pre-synaptic pulses (V_{pre}) and post-synaptic pulses (V_{post}) across the memristor, such that they arrive at two different instances in time, t_{pre} and t_{post}, respectively, with $\Delta t = t_{post} - t_{pre}$. The effective voltage across the memristor V_{eff} is given by: $V_{eff} = V_{post} - V_{pre}$. This is illustrated

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in Fig. 7(b). If the pre-synaptic pulse arrives before the post-synaptic pulse ($\Delta t > 0$), then the peak of V_{eff} is greater than the threshold value, and hence undergoes a potentiation (increasing conductance). If the pre-synaptic pulse arrives after the post-synaptic pulse ($\Delta t < 0$), then the peak of V_{eff} is below the threshold, and hence undergoes a depression (decreasing conductance).

B. Simulation results and discussion

In this section, the simulation of STDP behaviour in ECM-based Cu/MoS_2/Au memristors is explained using the proposed model. We have implemented this in Verilog-A; the simulation setup is shown in Fig. 7(c). A series of pre-synaptic and post-synaptic pulses are created using piecewise linear voltage source in Cadence Spectre, and are applied between the bottom and top electrodes of the memristor.

The simulation procedure is as follows. A post-synaptic pulse V_{post} is applied at the top electrode. Similarly, a pre-synaptic pulse V_{pre} is applied at the bottom electrode after a time delay. The pre-synaptic and post-synaptic pulses have the same shape, linearly increasing from $0V$ to $0.175V$ for a duration of $1ms$ and then from $-0.175V$ to $0V$ for a duration of $1ms$, arriving at two different time instances t_{pre} and t_{post}, respectively. Additionally, we have applied five pairs of such pre-synaptic and post-synaptic pulses, such that $|\Delta t| = 0.1, 0.3, 0.5, 0.7, 0.9ms$. Note that these inputs are consistent with the inputs used for the STDP measurement in the experimental setup detailed in [4].

The variation of these pre-synaptic (V_{pre}) and post-synaptic pulses (V_{post}), and the effective voltage across the memristor (V_{eff}) as a function of time, for $\Delta t < 0$ and $\Delta t > 0$, is shown in Fig. 7(d) and (e), respectively. We have calculated the conductance for each Δt value listed above, using the simulation procedure given in Fig. 2. For $\Delta t > 0$, the change in conductance is calculated from HRS. Similarly, for $\Delta t < 0$, the change in conductance is calculated from LRS [4]. Fig. 7(f) shows the change in conductance (ΔG) for different values of Δt, along with the corresponding value of the peak amplitude of the voltage across the memristor $|V_{eff}|$. The simulation results obtained using our model match well with the experimentally obtained data in [4].

For the simulation of neuromorphic applications aggregating these devices in a network, we should expect an inter-device dispersion. The inter-device variability in memristive neuromorphic systems has been experimentally analyzed in [62]. We have considered ten devices with different initial tunnel gaps ranging from $x_0 = 0.6L$ to $x_0 = L$, connected as shown in the inset of Fig. 8. The initial tunnel gaps of these devices are distributed, such that the difference in the tunnel gaps of these devices is about 0.5Å. The initial conductance of these devices are calculated using a read pulse of $0.1V$ and duration of $100\mu s$. Twenty consecutive SET (potentiation) pulses of magnitude $0.6V$ and duration $100\mu s$ are applied to all devices. Conductance is measured after each SET pulse, using a read voltage of magnitude $0.1V$ and duration $100\mu s$ as shown in the inset of Fig. 8. The observed conductance, and the estimated inter-device dispersion is shown in Fig. 8.

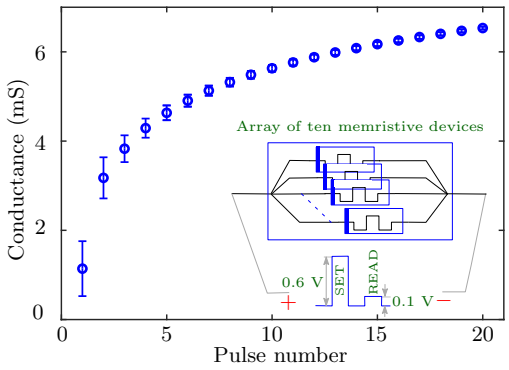

Fig. 8. Simulation results of variation in conductance as a function of consecutive pulses, for ten devices with different initial residual filament thickness. The error bar indicates the inter-device dispersion. The inset shows the simulation setup and the input signal.

Our simulation results show that the inter-device dispersion reduces with subsequent potentiation pulses. In ECM devices with remnant filaments, the height of the filament increases and becomes almost uniform in all devices as the number of consecutive potentiation pulses increase. Conductance in ECM devices mainly depends on the tunnel gap. Therefore, the inter-device dispersion in ECM devices decreases with repeated potentiation pulses.

Our model can be extended further, to estimate switching energies and to provide insight into the design of memristor arrays for neuromorphic applications.

VI. Conclusion

We have presented a one-dimensional model for filament growth, based on the physics of electrochemical metallization (implemented in Verilog-A) that captures the experimentally observed I-V characteristics, estimates multiple conductance states, and quantitatively captures the observed variability in the I-V characteristics, in 2D material-based ECM memristors with vertical transport. Our work demonstrates the flexibility of including different transport mechanisms (such as, tunneling, space charge limited conduction) in a unified simulation framework. The model is also able to capture the dynamics of switching (with an emphasis on the estimation of switching energies and delays), and is able to quantitatively capture the experimentally observed STDP behaviour in these devices. The simulation results have been validated with experimental data from multiple sources. Further, inter-device variability of 2D material-based ECM device has been analyzed using the proposed model. Our model can be extended to provide useful insight into the design of memristor crossbar architectures for neuromorphic and memory applications.

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